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04/15/98 jc588 U.S. PTO

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 42390.P5326 Total Pages 5

First Named Inventor or Application Identifier Scott L. Baker

Express Mail Label No. EM 542800080 US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 9)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 1)

4. X Oath or Declaration (Total Pages 4)
   a. X Newly Executed (Original or Copy)
   b. ___ Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ____ Microfiche Computer Program (Appendix)

7. __ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ____ Assignment Papers (cover sheet & documents(s))
9. ____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
__X__ b. Power of Attorney
10. ____ English Translation Document (if applicable)
11. __X__ a. Information Disclosure Statement (IDS)/PTO-1449
__X__ b. Copies of IDS Citations
12. ____ Preliminary Amendment
13. __X__ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. ____ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. ____ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. __X__ Other: Separate sheet with Certificate of mailing, attorney signature and registration number and copy of return postcard

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
___ Continuation ____ Divisional ____ Continuation-in-part (CIP)
of prior application No: _____

18. **Correspondence Address**
____ Customer Number or Bar Code Label _____
(Insert Customer No. or Attach Bar Code Label here)
or
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FEE TRANSMITTAL

TOTAL AMOUNT OF PAYMENT ($) $790.00

Complete if Known:
Application No.
Filing Date April 15, 1998
First Named Inventor Scott L. Baker
Group Art Unit
Examiner Name
Attorney Docket No. 42390.P5326

METHOD OF PAYMENT (check one)

1. [ ] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

   Deposit Account Number 02-2666
   Deposit Account Name

   [X] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

   [ ] Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance, 37 CFR 1.131(b)

2. X Payment Enclosed
   X Check
   Money Order
   Other

FEE CALCULATION (fees effective 10/01/97)

1. **FILING FEE**

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility application filing fee	$790.00
106	330	206	165	Design application filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional application filing fee	
				SUBTOTAL (1)	$ 790.00

2. **CLAIMS**

			Extra		Fee from below		Fee Paid
Total Claims	19	– 20 =	0	X		=	
Independent Claims	3	– 3 =	0	X		=	
Multiple Dependent Claims				X		=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
103	22	203	11	Claims in excess of twenty	
102	82	202	41	Independent claims in excess of 3	

104	270	204	135	Multiple dependent claim	
109	82	209	41	Reissue independent claims over original patent	
110	22	210	11	Reissue claims in excess of 20 and over original patent	

SUBTOTAL (2) $

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	400	216	200	Extension for response within second month	
117	950	217	475	Extension for response within third month	
118	1,510	218	755	Extension for response within fourth month	
128	2,060	228	1,030	Extension for response within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,320	241	660	Petition to revive unintentionally abandoned application	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	For filing a submission after final rejection (see 37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (see 37 CFR 1.129(a))	

Other fee (specify) _____

SUBTOTAL (3) _____

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: Aloysius T. C. AuYeung

Signature _____ Date 4/15/98

Reg. Number 35,432 Deposit Account User ID _____ (complete if applicable)

Express Mail Label: EM 542800080 US

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APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

METHOD AND APPARATUS FOR INTERLEAVING A DATA STREAM

Inventor(s): Scott L. Baker

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METHOD AND APPARATUS FOR INTERLEAVING A DATA STREAM

BACKGROUND

Field

The invention is related to interleaving data streams, such as binary data streams.

Background Information

In some situations it is desirable to have the capability to insert or remove groupings of bits or binary digital signals, such as, for example, from a data stream. It may also be desirable in some situations to interleave two separate data streams into a single data stream. One example, although not the only example, in which it is desirable to include the capability to insert or extract groupings of binary digital signals occurs in connection with virtual local area network (VLAN) tagging of binary digital signals, such as in an ethernet compliant system. VLAN tagging is being proposed as a recent addition to IEEE standard 802.1. See, for example, Draft Standard P802.1Q/D9, IEEE Standards for Local and Metropolitan Area Networks: Virtual Bridged Local Area Networks, available from the Institute of Electrical and Electronic Engineers, Inc. (IEEE), 345 East 47th Street, New York, N.Y., 10017.

SUMMARY

Briefly, in accordance with one embodiment of the invention, a method of interleaving a data stream may occur as follows. A sequence of groupings of bits or binary digital signals from a data stream, the groupings have a predetermined size, are written from a data bus into a memory. Selective groupings stored in the memory are applied to a first multiplexer (MUX). Groupings applied to the first MUX are then applied to a second MUX. At least one grouping, applied to a third MUX, is applied to the second MUX between applying groupings from the first MUX to the second MUX.

Briefly, in accordance with another embodiment of the invention, an integrated circuit includes: a memory, a plurality of multiplexers, and a state machine. The memory, multiplexers and state machine are coupled so that selected groupings of bits from the received bit stream are capable of being extracted to produce another bit stream different from the received bit stream.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features, and advantages thereof,

may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

FIG. 1 is a block diagram illustrating an embodiment of a circuit for interleaving a data stream.

DETAILED DESCRIPTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have been described in detail so as not to obscure the present invention.

It is sometimes desirable to insert and/or remove consecutive binary digital signals, referred to in this context as groupings of bits, from a data stream. Likewise, although the invention is not limited in scope in this respect, it may be desirable to interleave two data streams to form a single data stream. In yet another example, although, again the invention is not limited in scope in this respect, it may be desirable to insert or remove a virtual local area network (VLAN) tag from a data stream, such as in the context of an ethernet switch or similar device, for example. VLAN tagging is being proposed as a recent addition to IEEE standard 802.1. VLAN tags are described, for example, in Draft Standard P802.1Q/D9, IEEE Standards for Local and Metropolitan Area Networks: Virtual Bridged Local Area Networks, available from the Institute of Electrical and Electronic Engineers, Inc. (IEEE), 345 East 47th Street, New York, N.Y., 10017.

FIG. 1 is a block diagram illustrating an embodiment of a circuit for interleaving a data stream in accordance with the present invention. This circuit may be embodied on an integrated circuit, although the invention is not limited in scope in this respect. Likewise, a system may include a personal computer (PC) adapted to be coupled to an ethernet compliant network, for example. Although the invention is not limited in scope in this respect, this system may include an integrated circuit including the embodiment illustrated in FIG. 1. As illustrated in FIG. 1, binary digital signals or bits traverse a data bus 185. In this particular embodiment, a sequence of groupings of bits from a data stream are received and written from data bus 185 into memory 110. In this particular embodiment, the groupings have a predetermined size, such as a byte, although the invention is not limited in scope in this respect. In this particular embodiment, although the invention is not limited in scope in this respect, memory 110 comprises a first-in,

first-out memory (FIFO). As illustrated in FIG. 1, FIFO memory 110 includes a FIFO read pointer 105 and a FIFO write pointer 115. These may be employed to write received groupings of bits from the data stream into the FIFO memory and to read groupings of bits from the FIFO memory and apply them to MUX 120, as shall be explained in more detail hereinafter.

As illustrated in FIG. 1, the read and write pointers of FIFO 110 may be employed to effectively skip or extract received groupings of bits from the data stream that has been stored in the FIFO. For example, once a grouping of binary digital signals, for example, a byte, has been written to FIFO 110, read pointer 105 may skip that grouping so that it is not read from FIFO 110 and applied to MUX 120. As illustrated in FIG. 1, a state machine 150 provides the signals to FIFO read pointer 105 so that this extraction operation may be accomplished. Likewise, as illustrated, state machine 150 also provides signals to MUX ports 125, 135, 145 as well, to ensure that the operations occurring at MUXes 120, 130 and 140 are coordinated with the operation of FIFO 110 when this extraction operation is performed. It will, of course, be appreciated that a variety of digital circuits may be employed to perform the operation of state machine 150 and, therefore, the invention is not limited in scope to a particular type of circuitry or a particular state machine. As previously described, selected groupings of bits from the data stream, stored in the FIFO, are read from the FIFO or applied to MUX 120. As illustrated in FIG. 1, in this particular embodiment, this operation is performed a grouping at a time. Therefore, a grouping of binary digital signals, such as a byte, is applied to MUX 120, all the bits being applied to input ports of the MUX substantially simultaneously. One advantage of employing this approach, although the invention is not limited in scope in this respect, is that it allows the use of a slower speed FIFO while supporting a high output clock rate. More particularly, although bits may be received at a relatively high rate by a data bus 185, because groupings of bits are read from FIFO 110, more time separates read operations, permitting a relatively slower memory.

In addition to the extraction operation previously described, this particular embodiment of a circuit for interleaving a data stream includes the capability to interleave a grouping or groupings of binary digital signals. In this particular embodiment, this capability is provided via the arrangement between MUXes 120, 135 and 145, as explained in more detail hereinafter. As illustrated in FIG. 1, the output data stream is produced at output port 165 of MUX 140. Signals are applied to the input ports of MUX, 140 in this particular embodiment, from the output ports of MUXes 120 and 130, respectively. Likewise, a signal applied to MUX select port 145 of MUX 140 controls which of the input signals applied to MUX 140 appears at its output port 165.

In this particular embodiment, MUX 130 receives input signals from an alternative data source. This data source or data stream is to be interleaved with the data stream written to FIFO

110, as previously described. Therefore, a signal applied to MUX select port 135 of MUX 130 controls the application of signals from this alternative data source or data stream to MUX 140. Likewise, selective groupings stored in FIFO 110 may be applied to the input port of 140 via MUX 120 by the application of a control signal to MUX select port 125 of MUX 120. Therefore, as previously illustrated, in this particular embodiment, controlling the signals applied MUX select ports 125, 135 and 145 of MUXes 120, 130 and 140 may result in the interleaving of the data stream written to FIFO 110 and the data stream applied to MUX 130. Although the invention is not limited in scope in this respect, the alternative data stream or data source applied to MUX 130 may comprise bits of binary digital signals representing a VLAN tag, for example. Therefore, this tag may be interleaved with the data signals with FIFO 110, as a data stream is produced by output port 165.

In one embodiment, although the invention is not limited in scope in this respect, binary digital signals may be received via data bus 185 and written to FIFO 110 in bursts of data signals. For example, although the invention is not limited in scope in this respect, a dynamic random access memory (DRAM) may be coupled to data bus 185 and provide these bursts of bits or binary digital signals.

An embodiment of a method of interleaving a data stream in accordance with the invention may be accomplished as follows. A sequence of groupings of bits from a data stream may be written from a data bus into memory. For example, as illustrated in FIG. 1, with databus 185 and memory 110. The groupings in this embodiment have a predetermined size. Selected groupings that are stored in the memory may be read from it and applied to a first multiplexer (MUX). Again, this is illustrated in FIG. 1 by MUX 120. The groupings applied to the first MUX are then applied to the second MUX, in this embodiment, by the first MUX. However, at least one grouping is applied to the second MUX between applying the groupings from the first MUX to the second MUX.

If FIG. 1, this is accomplished with MUXes 140 and 130. If the at least one grouping is from a data stream, then this embodiment provides a method of interleaving the data streams for the embodiment illustrated in FIG. 1, the memory comprises a first-in, first-out memory (FIFO). Likewise, the sequence of groupings of bits are received consecutively, via a data bus in this embodiment, as previously indicated, and written into memory. The grouping size may comprise a byte in one embodiment. One of the groupings may comprise a virtual local area network (VLAN) tag. Also, the data signals may be provided in bursts, such as from a burst node dynamic modem access memory (DRAM), for example. Of course, the invention is not limited in scope to the features of this particular embodiment.

While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

Claims:

1. A method of interleaving a data stream comprising:

writing a sequence of groupings of bits from the data stream, the groupings having a predetermined size, from a data bus into a memory;

applying selected groupings read from the memory to a first multiplexer (MUX);

applying the groupings applied to the first MUX to a second MUX; and

applying at least one grouping to the second MUX between applying groupings from the first MUX to the second MUX.

2. The method of claim 1, wherein the memory comprises a first-in, first-out memory (FIFO).

3. The method of claim 1, wherein each of the groupings comprises a byte.

4. The method of claim 1, wherein said at least one grouping comprises bits representing a virtual local area network (VLAN) tag.

5. The method of claim 4, wherein said at least one grouping comprises bits originating from another data stream.

6. The method of claim O-1, wherein writing a sequence of groupings of bits into a memory comprises receiving a consecutive sequence of groupings of bits and writing the consecutive sequence into the memory.

7. The method of claim 6, wherein receiving a consecutive sequence of groupings of bits and writing the consecutive sequence into the memory comprises receiving bursts of data signals and writing the received bursts of data signals to the memory.

8. The method of claim 6, wherein the bursts of data signals are provided via the data bus from at least one burst-mode memory.

9. The method of claim 8, wherein the at least one burst mode memory comprises at least one burst mode dynamic random access memory (DRAM).

10. The method of claim 1, wherein applying selected groupings read from the memory to a first MUX comprises selecting, from the stored groupings, groupings that represent signal information other than a virtual local area network (VLAN) tag.

11. The method of claim 1, wherein applying groupings read from memory to the first MUX occurs a grouping at a time.

12. An integrated circuit (IC) comprising:

a memory, a plurality of multiplexers (MUXes), and a state machine;

said memory, MUXes and state machine being coupled so that, responsive to applied control signals, selected groupings of bits from a received bit stream are capable of being extracted to produce another bit steam different from the received bit stream.

13. The IC of claim 12, wherein said state machine comprises a memory extraction state machine.

14. The IC of claim 12, wherein said memory comprises a first-in, first-out memory (FIFO).

15. The IC of claim 12, wherein said memory and MUXes are further coupled so that, responsive to additional applied control signals, at least one selected grouping from another data stream may be inserted to produce a bit stream different from the received bit stream.

16. The IC of claim 15, wherein said memory comprises a first-in, first-out memory (FIFO), and said state machine comprises a FIFO extraction state machine.

17. The IC of claim 15, wherein said memory is adapted to receive said received bit stream in bursts of data signals.

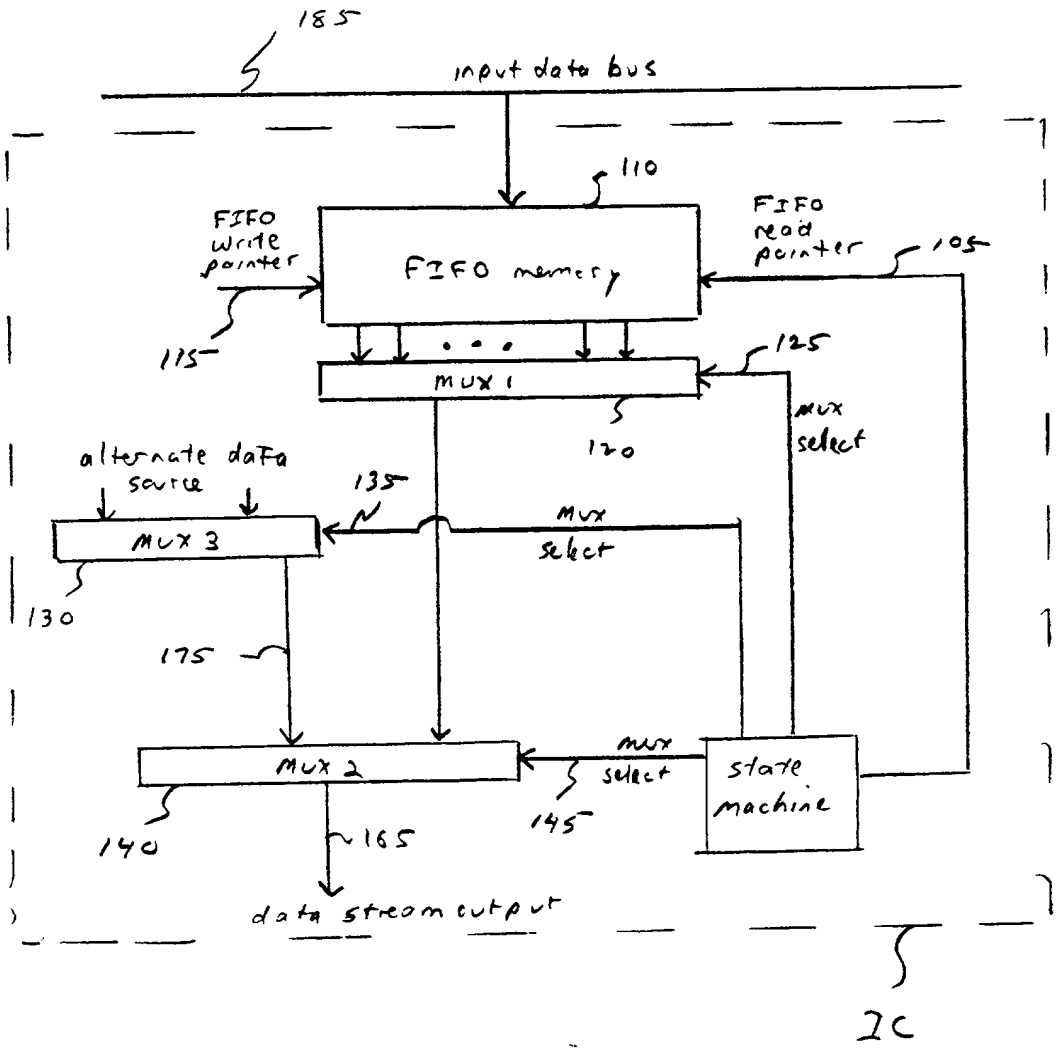
18. A system comprising: a computer adapted to be coupled to an ethernet compliant network; said computer including an integrated circuit; the integrated circuit comprising a memory, a plurality of multiplexers (MUXes) and a state machine; said memory, MUXes, and state machine being coupled so that, responsive to applied control signals, selected groupings of bits from a received bit stream are capable of being extracted to produce another bit stream different from the received bit stream.

19. The system of claim 18, wherein said memory and MUXes are further coupled, so that, responsive to additional control signals, at least one selected grouping from another data stream may be inserted to produce yet another bit stream different from the received bit stream.

ABSTRACT

Briefly, in accordance with one embodiment of the invention, a method of interleaving a data stream may occur as follows. A sequence of groupings of bits or binary digital signals from a data stream, the groupings have a predetermined size, are written from a data bus into a memory. Selective groupings stored in the memory are applied to a first multiplexer (MUX). Groupings applied to the first MUX are then applied to a second MUX. At least one grouping, applied to a third MUX, is applied to the second MUX between applying groupings from the first MUX to the second MUX.

Briefly, in accordance with another embodiment of the invention, an integrated circuit includes: a memory, a plurality of multiplexers, and a state machine. The memory, multiplexers and state machine are coupled so that selected groupings of bits from the received bit stream are capable of being extracted to produce another bit stream different from the received bit stream.



100

FIG. 1

P5326

Sheet 1 of 1

Attorney's Docket No.: 42390.P5326 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD AND APPARATUS FOR INTERLEAVING A DATA STREAM

the specification of which

_X_ is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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